**COMP 2601**

**Tutorial 5**

1. The following machine instructions are to be executed on a computer with an instruction pipeline with four stages: FI- instruction fetch, DI – decode instruction, FO - fetch operand and EI – execute instruction.

010 add r6, r6, r4

011 ld r1, A

012 add r1, r1, 1

013 blt r1, r6, 500

014 add r3, r3, r4

015 sub r5, r5, r2

…

*blt is a conditional branch instruction: if (r1) < (r6) then jump to instruction address 500*

* 1. Draw a timing diagram for the above sequence of instructions and illustrate the types of hazards that prevent the pipeline from giving optimal performance.
  2. Use noops to rewrite the sequence of instructions so that the pipeline can run without stopping.

1. A non-pipelined processor (with a clock rate of 1 GHz) was upgraded to a processor (with a clock rate of 2.5 GHz) that supports an instruction pipeline with stages:

I – instruction fetch

E1 – register read

E2 – ALU operation and register write

D – memory access for a load (memory to register) or store (register to memory) operation.

A separate instruction cache and data cache is maintained by the hardware.

* 1. Use a sequence of generic assembly instructions and a timing diagram to explain how a data hazard and a control hazard can occur in the instruction pipeline.
  2. Calculate the expected speedup when a program of 100,000 machine instructions are executed on the pipelined processor compared to the non-pipelined processor. Assume that instructions are issued at the rate of one per clock cycle on both processors.

1. Assume a pipeline with 4 stages:

FI – fetch instruction

DA – decode and calculate address

FO – fetch operand

EX – execute

Draw a timing diagram for a sequence of 7 instructions, in which the third instruction is a branch that is taken and in which there are no data dependencies.

1. A pipelined processor has a clock rate of 2.5 GHz and executes a program with 1.5 million instructions. The pipeline has 5 stages, and instructions are issued at a rate of one per clock cycle. Ignore the penalties due to branch instructions and out-of-sequence executions.
   1. What is the speedup of this processor for this program compared to a non-pipelined processor? Make the same assumptions as those used in determining pipelining performance.
   2. What is the throughput (in MIPS – Millions of Instructions Per Second) of the pipelined processor?
2. A microprocessor is clocked at a rate of 5 GHz.
   1. How long is a clock cycle?
   2. What is the duration of a particular type of machine instruction consisting of three clock cycles?
3. A microprocessor provides an instruction capable of moving a string of bytes from one area of memory to another. The fetching and initial decoding of the instruction takes 10 clock cycles. Thereafter, it takes 15 clock cycles to transfer each byte. The microprocessor is clocked at a rate of 10 GHz.
   1. Determine the length of the instruction cycle for the case of a string of 64 bytes.
   2. What is the worst-case delay for acknowledging an interrupt if the instruction is non-interruptible?
   3. Repeat part (b) assuming the instruction can be interrupted at the beginning of each byte transfer.
4. If the last operation performed on a computer with an 8-bit word was an addition in which the two operands were 00000010 and 00000011, what would be the value of the following flags?
   1. Carry, Zero, Overflow, Sign, Even Parity
   2. Repeat for the addition of -1 (twos complement) and +1.
   3. Name 2 general roles of registers
   4. What is a PSW?
   5. List and briefly explain the various ways in which an instruction pipeline can deal with conditional branch instructions.
   6. How are history bits used for branch predictions?
   7. Why is a two-stage instruction pipeline unlikely to cut the instruction cycle time in half, compared with the use of no pipeline?